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(54) **ELECTROLUMINESCENT DISPLAY DEVICE**

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(57) **ABSTRACT**

Disclosed is an electroluminescent display device capable of overcoming a problem related with a resistance of a low level voltage line without any loss of an aperture ratio, wherein the electroluminescent display device may include a substrate, a first electrode provided on the substrate, a bank configured to cover an end of the first electrode and to define an emission area, an emission layer provided on the first electrode in the emission area defined by the bank, a second electrode provided on the emission layer and the bank, a conductive layer provided on the second electrode, and the low level voltage line provided on the substrate and electrically connected with the second electrode or the conductive layer.

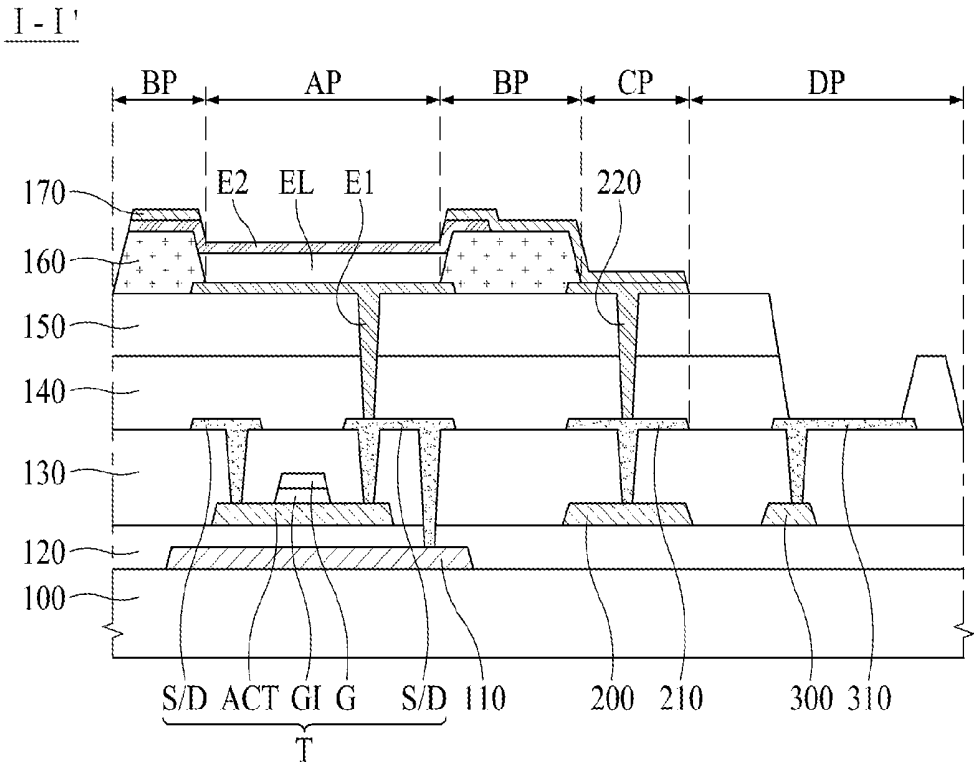


FIG. 1

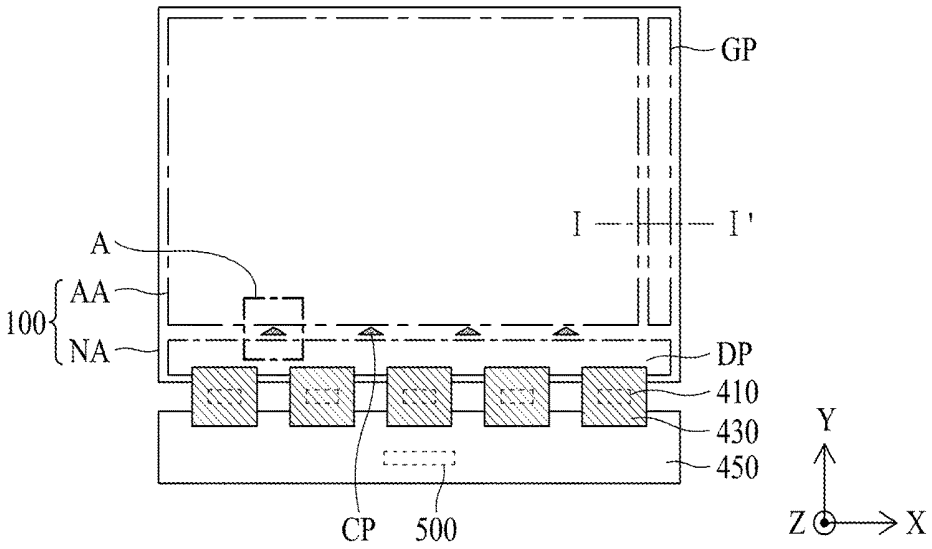

GP
I
I'
A
AA
100
NA
DP
410
430
450
CP
500
Y
Z
X

FIG. 2

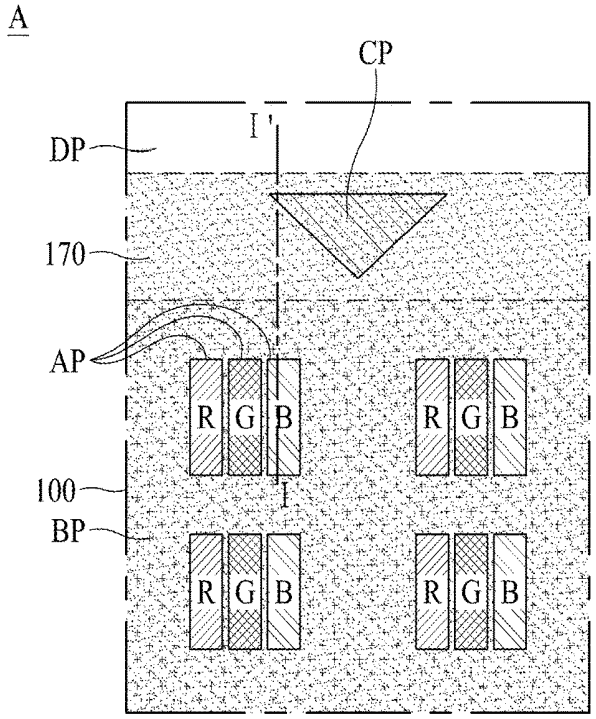

A
CP
I'
DP
170
AP
R
G
B
100
BP

FIG. 3

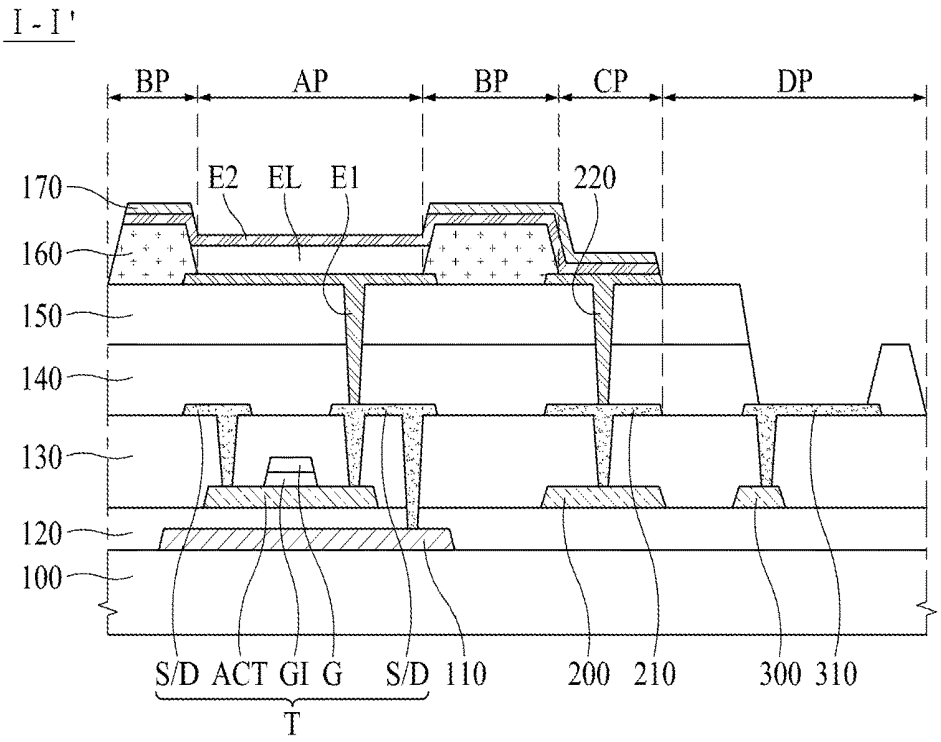
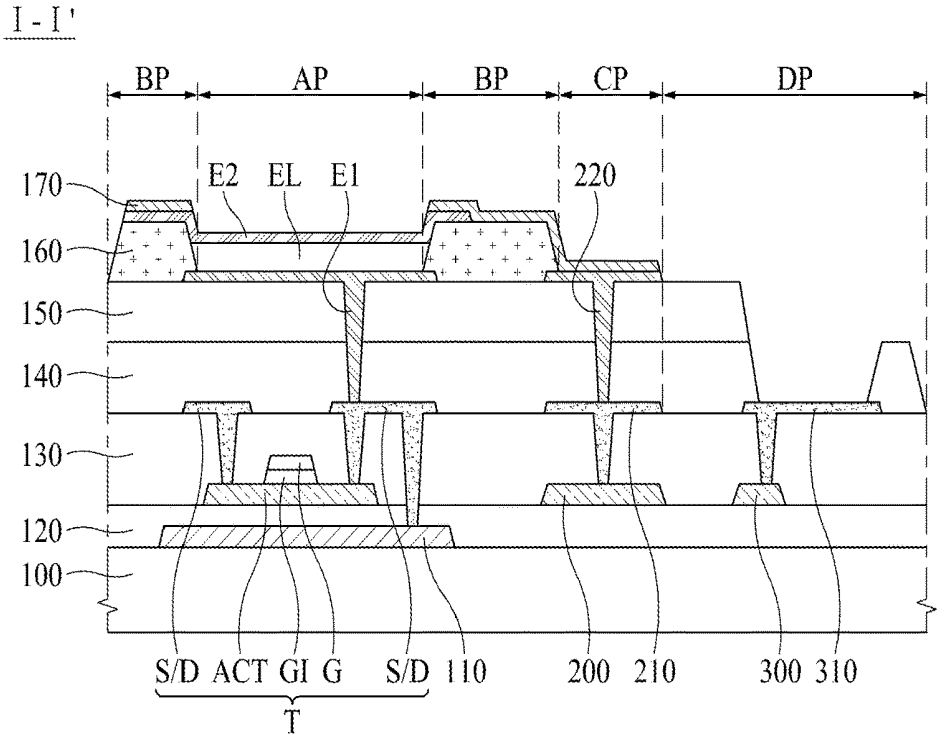

I - I'
BP
AP
BP
CP
DP
170
160
150
140
130
120
100
E2
EL
E1
220
S/D
ACT
GI
G
S/D
110
200
210
300
310
T

FIG. 4


I - I'
BP
AP
BP
CP
DP
170
160
150
140
130
120
100
E2
EL
E1
220
S/D
ACT
GI
G
S/D
110
200
210
300
310
T

ELECTROLUMINESCENT DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the Korean Patent Application No. 10-2017-0184839 filed on Dec. 29, 2017, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND

Technical Field

[0002] The present disclosure relates to an electroluminescent display device.

Description of the Related Art

[0003] An electroluminescent display device is provided in such way that an emission layer is formed between two electrodes. According as the emission layer emits light by an electric field generated between the two electrodes, an image is displayed on the electroluminescent display device.

[0004] The emission layer may be formed of an organic material which emits light when the exciton is produced by a bond of electron and hole, and the exciton falls to a ground state from an excited state. Otherwise the emission layer may be formed of an inorganic material such as quantum dot.

[0005] Recently, a top emission type is applied to the electroluminescent display device. Most cases of the top emission type of the electroluminescent display device, a cathode electrode is provided with a thin thickness and formed of a transparent metal material. Accordingly, the low level voltage line connected with the cathode electrode is increased in its resistance so that it may cause a problem related with non-uniformity of luminance over all pixels.

SUMMARY

[0006] The present disclosure has been made in view of the above problems, and it is an object of the present disclosure to provide an electroluminescent display device which is capable of overcoming a problem related with a resistance of the low level voltage line without any loss of an aperture ratio.

[0007] In accordance with an aspect of the present disclosure, the above and other objects can be accomplished by the provision of an electroluminescent display device comprising a substrate, a first electrode provided on the substrate, a bank configured to cover an end of the first electrode and to define an emission area, an emission layer provided on the first electrode in the emission area defined by the bank, a second electrode provided on the emission layer and the bank, a conductive layer provided on the second electrode, and the low level voltage line provided on the substrate and electrically connected to the second electrode or the conductive layer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0008] The above and other objects, features and other advantages of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0009] FIG. **1** is a plane view illustrating an electroluminescent display device according to one embodiment of the present disclosure;

[0010] FIG. **2** is an enlarged plane view showing rectangular portion 'A' of FIG. **1**;

[0011] FIG. **3** is a cross sectional view along I-I' of FIG. **2** according to the first embodiment of the present disclosure; and

[0012] FIG. **4** is a cross sectional view along I-I' of FIG. **2** according to the second embodiment of the present disclosure.

DETAILED DESCRIPTION DISCLOSURE

[0013] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through the following embodiments, described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art. Further, the present disclosure is only defined by the scope of the claims.

[0014] The shapes, sizes, ratios, angles, and numbers disclosed in the drawings for describing embodiments of the present disclosure are merely examples, and thus the present disclosure is not limited to the illustrated details. Like reference numerals refer to like elements throughout. In the following description, when the detailed description of the relevant known function or configuration is determined to unnecessarily obscure the important point of the present disclosure, the detailed description will be omitted.

[0015] In the case in which "comprise," "have," and "include" described in the present specification are used, another part may also be present unless "only" is used. The terms in a singular form may include plural forms unless noted to the contrary.

[0016] In construing an element, the element is construed as including the margins of error although there is no explicit description thereof.

[0017] In describing a positional relationship, for example, when the positional order is described as "on," "above," "below," and "next," the case of no contact therebetween may be included, unless "just" or "direct" is used. If it is mentioned that a first element is positioned "on" a second element, it does not mean that the first element is essentially positioned above the second element in the figure. The upper part and the lower part of an object concerned may be changed depending on the orientation of the object. Consequently, the case in which a first element is positioned "on" a second element includes the case in which the first element is positioned "below" the second element as well as the case in which the first element is positioned "above" the second element in the figure or in an actual configuration.

[0018] In describing a temporal relationship, for example, when the temporal order is described as "after," "subsequent," "next," and "before," a case which is not continuous may be included, unless "just" or "direct" is used.

[0019] It will be understood that, although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element

from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure.

[0020] The terms "first horizontal axis direction," "second horizontal axis direction," and "vertical axis direction" should not be interpreted only based on a geometrical relationship in which the respective directions are perpendicular to each other, and may be meant as directions having wider directivities within the range within which the components of the present disclosure can operate functionally.

[0021] It should be understood that the term "at least one" includes all combinations related with any one item. For example, "at least one among a first element, a second element and a third element" may include all combinations of two or more elements selected from the first, second and third elements as well as each element of the first, second and third elements.

[0022] Features of various embodiments of the present disclosure may be partially or overall coupled to or combined with each other, and may be variously inter-operated with each other and driven technically as those skilled in the art can sufficiently understand. The embodiments of the present disclosure may be carried out independently from each other, or may be carried out together in a co-dependent relationship.

[0023] Hereinafter, an electroluminescent display device according to the embodiment of the present disclosure will be described in detail with reference to the accompanying drawings.

[0024] FIG. **1** is a plane view illustrating an electroluminescent display device according to one embodiment of the present disclosure. In FIG. **1**, an X-axis indicates a direction which is parallel to a gate line, a Y-axis indicates a direction which is parallel to a data line, and a Z-axis indicates a height (or thickness) direction of the electroluminescent display device.

[0025] Referring to FIG. **1**, the electroluminescent display device according to one embodiment of the present disclosure may include a substrate **100**, a source drive integrated circuit **410**, a flexible film **430**, a circuit board **450** and a timing controller **500**.

[0026] The substrate **100** may be a flexible substrate. For example, the substrate **100** may include a transparent polyimide material. The substrate **100** of the polyimide material may be obtained by curing polyimide resin coated in a constant thickness onto a front surface of a release layer prepared in a carrier glass substrate. The carrier glass substrate is separated from the substrate **100** by the elimination of the release layer for a laser release process. On one surface of the substrate **100**, there are gate lines, data lines, and pixels. The pixels may include a plurality of sub pixels, and the plurality of sub pixels are provided adjacent to crossing areas of the gate lines and the data lines.

[0027] The substrate **100** according to one embodiment of the present disclosure may include an active area AA and a non-active area NA.

[0028] The active area AA corresponds to an area for displaying an image thereon, which may be defined in the middle of the substrate **100**. The active area AA may be provided with the gate lines, the data lines and the pixels.

[0029] The non-active area NA corresponds to an area on which an image is not displayed, wherein the non-active area NA may be defined in the periphery of the substrate **100** so as to surround the active area AA. The non-active area NA may be provided with a gate driver GP, a pad portion DP and a low level voltage line contact portion CP.

[0030] The gate driver GP supplies the gate signals to the gate lines in accordance with a gate control signal which is provided from the timing controller **500**. The gate driver GP may be provided in the non-active area NA at an outer side of the active area AA of the substrate **100** by a GIP (gate driver in panel) method.

[0031] The pad portion DP supplies the data signals to the data lines in accordance with a data control signal which is provided from the timing controller **500**. The pad portion DP may be manufactured in a driving chip, mounted on the flexible film **430**, and attached to the non-active area NA at an outer area from the active area AA of the substrate **100** by a TAB (tape automated bonding) method.

[0032] The low level voltage line contact portion CP may connect a low level voltage line and a second electrode included in the pixel of the active area AA. For example, the low level voltage line contact portion CP is provided in an area which is overlapped with the edge of the second electrode, whereby the low level voltage line contact portion CP may be electrically connected to the edge of the second electrode via a contact hole.

[0033] The source drive integrated circuit **410** receives the digital video data and the source control signal from the timing controller **500**. The source drive integrated circuit **410** converts the digital video data into the analog data voltages in accordance with the source control signal, and provides the analog data voltages to the data lines. If the source drive integrated circuit **410** is manufactured in a driving chip, the source drive integrated circuit **410** may be mounted on the flexible film **430** by a COF (chip on film) or COP (chip on plastic) method.

[0034] The flexible film **430** may be provided with lines for connecting the pad portion DP and the source drive integrated circuit **410** with each other, and lines for connecting the pad portion DP and the circuit board **450** with each other. The flexible film **430** is attached onto the pad portion DP by the use of anisotropic conducting film, whereby the pad portion DP may be connected to the lines of the flexible film **430**.

[0035] The circuit board **450** may be attached to the flexible films **430**. A plurality of circuits, which are embodied in driving chips, may be mounted on the circuit board **450**. For example, the timing controller **500** may be mounted on the circuit board **450**. The circuit board **450** may be a printed circuit board or a flexible printed circuit board.

[0036] The timing controller **500** receives the digital video data and the timing signal from an external system board via a cable of the circuit board **450**. The timing controller **500** generates a gate control signal for controlling an operation timing of the gate driver GP, and a source control signal for controlling the source drive integrated circuits **410** on the basis of timing signal. The timing controller **500** supplies the gate control signal to the gate driver GP, and supplies the source control signal to the source drive integrated circuits **410**.

[0037] FIG. **2** is an enlarged plane view showing rectangular portion 'A' of FIG. **1**. FIG. **3** is a cross sectional view along I-I' of FIG. **2** according to the first embodiment of the present disclosure.

[0038] Referring to FIGS. **2** and **3**, the electroluminescent display device according to the first embodiment of the

present disclosure may include a substrate **100**, a light shielding layer **110**, a buffer layer **120**, a thin film transistor T, an insulating interlayer **130**, a passivation layer **140**, a planarization layer **150**, a first electrode E**1**, a bank **160**, an emission layer EL, a second electrode E**2**, a conductive layer **170**, a low level voltage line (VSS) **200**, a signal pad **300** and a pad electrode **310**.

[0039] The substrate **100** may be a flexible substrate, as described above, but not limited to this type.

[0040] As described above, the substrate **100** according to one embodiment of the present disclosure may include an active area AA and a non-active area NA, wherein the active area AA may include a aperture portion AP and a bank portion BP, and the non-active area NA may include a gate driver GP, a pad portion DP and a low level voltage line contact portion CP.

[0041] The aperture portion AP may be an emission portion which is not provided with a bank, and the bank portion BP may be a non-emission portion which is provided with a bank. As described above, the gate driver GP, the pad portion DP and the low level voltage line contact portion CP correspond to the predetermined portions of the non-active area NA. However, elements for the non-active area NA are not limited to the above portions such as the gate driver GP, the pad portion DP and the low level voltage line contact portion CP, that is, the non-active area NA is not realized by combining only the above portions such as the gate driver GP, the pad portion DP and the low level voltage line contact portion CP.

[0042] The light shielding layer **110** is provided on the aperture portion AP of the substrate **100**. The light shielding layer **110** prevents light from being advanced to an active layer ACT to be explained later.

[0043] The buffer layer **120** is provided on the light shielding layer **110**. The buffer layer **120** extends from the active area AA to the non-active area NA. The buffer layer **120** may be formed of an inorganic insulating material, for example, formed in a singular-layered structure or a multi-layered structure of silicon oxide (SiOx) film or silicon nitride (SiNx) film, but not limited to these structures.

[0044] The thin film transistor T is provided on the aperture portion AP of the substrate **100**. And more particularly, the thin film transistor T is provided on the buffer layer **120**. The thin film transistor T may include the aforementioned active layer ACT, a gate electrode G, and source/drain electrodes S/D.

[0045] The active layer ACT is provided on the buffer layer **120**. A gate insulating film GI is provided on the active layer ACT, and a gate electrode G is provided on the gate insulating film GI. Further, an intermediate insulating interlayer **130** is provided on the gate electrode G, and the source/drain electrodes S/D are provided on the insulating interlayer **130**.

[0046] The active layer ACT according to one embodiment of the present disclosure may be formed of a silicon-based semiconductor material or oxide-based semiconductor material.

[0047] The gate insulating film GI insulates the active layer ACT and the gate electrode G from each other, wherein a pattern of the gate insulating film GI may be identical to a pattern of the gate electrode G. The gate insulating film GI may be formed of an inorganic insulating material, for example, formed in a singular-layered structure or a multi-layered structure of silicon oxide (SiOx) film or silicon nitride (SiNx) film, but not limited to these structures.

[0048] The gate electrode G is provided on the gate insulating film GI.

[0049] The intermediate insulating interlayer **130** may be formed of an inorganic insulating material, for example, formed in a singular-layered structure or a multi-layered structure of silicon oxide (SiOx) film or silicon nitride (SiNx) film, but not limited to these structures. The intermediate insulating interlayer **130** extends from the active area AA to the non-active area NA.

[0050] The source/drain electrodes S/D confronting each other are provided on the insulating interlayer **130**. Herein, contact holes for exposing one end and the other end of the active layer ACT are provided in the intermediate insulating interlayer **130**, and the source/drain electrodes S/D are respectively connected with one end and the other end of the active layer ACT via the contact holes.

[0051] In addition, a contact hole for exposing the light shielding layer **110** is provided in the buffer layer **120** and the intermediate insulating interlayer **130**, and the source/drain electrodes S/D are connected with the light shielding layer **110** via the contact hole. The light shielding layer **110** according to one embodiment of the present disclosure is formed of a conductive material. When the light shielding layer **110** is in the floating state, the active layer ACT may be negatively influenced by the floating light shielding layer **110**. In this reason, the light shielding layer **110** is connected with the source/drain electrodes S/D so that it is possible to prevent any adverse influence or effect on the active layer ACT.

[0052] The passivation layer **140** is provided on the source/drain electrodes S/D. The passivation layer **140** protects the thin film transistor T, and the passivation layer **140** extends from the active area AA to the non-active area NA. The passivation layer **140** may be formed of an inorganic insulating material, for example, silicon oxide (SiOx) film or silicon nitride (SiNx) film, but not limited to these materials.

[0053] The planarization layer **150** is provided on the passivation layer **140**. The planarization layer **150** may be configured to planarize an upper surface of the substrate **100** including the thin film transistor T. The planarization layer **150** may be formed of an organic insulating material, for example, acryl resin, epoxy resin, phenolic resin, polyamide resin, polyimide resin, and etc., but not limited to these materials.

[0054] The first electrode E**1** is provided within the aperture portion AP of the substrate **100**. The first electrode E**1** is provided on the planarization layer **150**.

[0055] The first electrode E**1** according to one embodiment of the present disclosure may be connected to the source electrode S or the drain electrodes D via the contact hole provided in the passivation layer **140** and the planarization layer **150**.

[0056] The first electrode E**1** according to one embodiment of the present disclosure is patterned as corresponding to each pixel, and the first electrode E**1** according to one embodiment of the present disclosure may serve as an anode of the electroluminescent display device. When the electroluminescent display device according to one embodiment of the present disclosure is applied to a top emission type, the first electrode E**1** may include a reflective material for upwardly reflecting light emitted from the emission layer EL. In this case, the first electrode E**1** may be formed in a

stacked structure including the reflective material and a transparent conductive material.

[0057] The bank **160** is provided on the bank portion BP of the substrate **100**. The bank **160**, which covers an end of the first electrode E**1**, is configured to define an emission area. An upper surface of the first electrode E**1** is exposed in the emission area between each of the banks **160** according to one embodiment of the present disclosure, and light is emitted through the exposed upper surface of the first electrode E**1**, to thereby display an image.

[0058] The bank **160** according to one embodiment of the present disclosure may be formed of an organic insulating material, for example, polyimide resin, acryl resin, benzocyclobutene (BCB), and etc., but not limited to these materials.

[0059] The emission layer EL is provided on the aperture portion AP of the substrate **100**. The emission layer EL is provided on the first electrode E**1** in the emission area defined by the bank **160**. The emission layer EL according to one embodiment of the present disclosure may include a hole injecting layer, a hole transporting layer, an organic emitting layer, an electron transporting layer, and an electron injecting layer. The structure of the emission layer EL may be changed in various types generally known to those in the art.

[0060] The emission layer EL according to one embodiment of the present disclosure may include a red emitting material layer, a green emitting material layer and a blue emitting material layer. Accordingly, the aperture portion AP may include a red sub pixel, a green sub pixel and a blue sub pixel, wherein the above red, green and blue sub pixels constitute one unit pixel.

[0061] The second electrode E**2** is provided on the emission layer EL and the bank **160**. In the case of the top emission type, as the second electrode E**2** is provided on a light emission surface, the second electrode E**2** is preferably formed of a transparent conductive material. However, as the transparent conductive material has a high resistance, the conductive layer **170** may be additionally provided so as to reduce the resistance of the second electrode E**2**.

[0062] The second electrode E**2** according to one embodiment of the present disclosure may be provided on the active area AA and the low level voltage line contact portion CP of the substrate **100**. In detail, the second electrode E**2** may be provided to cover the active area AA and the low level voltage line contact portion CP of the substrate **100** as one body. Accordingly, the second electrode E**2** is provided as one body without being patterned by each pixel, and the second electrode E**2** is thinly formed of a transparent conductive material, for example, metal material such as MgAg, whereby the low level voltage line **200** electrically connected with the second electrode E**2** may have a high resistance, and it may cause non-uniformity of luminance over all of the pixels. Thus, the electroluminescent display device according to the first embodiment of the present disclosure may include the conductive layer **170**, additionally.

[0063] The conductive layer **170** is provided on the second electrode E**2**. The conductive layer **170** is in contact with the second electrode E**2** so that it is possible to reduce the resistance of the second electrode E**2**. The conductive layer **170** is provided on the bank portion BP and the low level voltage line contact portion CP of the substrate **100**.

[0064] The conductive layer **170** according to one embodiment of the present disclosure may be formed of a metal material having high conductivity, for example, aluminum (Al). The conductive layer **170** is formed in a pattern shape on the bank portion BP and the low level voltage line contact portion CP so that it is possible to prevent transmittance of the aperture portion AP from being deteriorated. As the conductive layer **170** is formed of the material having high conductivity, it is possible to reduce the resistance of the second electrode E**2** through the surface contact between the conductive layer **170** and the second electrode (E**2**).

[0065] The conductive layer **170** according to one embodiment of the present disclosure may be formed of a reflective material. In this case, light emitted from the emission layer EL may be reflected on the conductive layer **170** so that it is possible to improve a light emission efficiency.

[0066] Meanwhile, although not shown in figures, an encapsulation layer may be additionally provided on the conductive layer **170** so as to prevent external moisture or oxygen from being permeated into the emission layer EL. The encapsulation layer may be formed of an inorganic insulating material, or may be formed in a stacked structure obtained by alternately depositing an inorganic insulating material and an organic insulating material, but not limited to these structures.

[0067] The low level voltage line **200** is provided on the low level voltage line contact portion CP of the substrate **100**. The low level voltage line **200** is provided on the buffer layer **120**. The low level voltage line **200** according to one embodiment of the present disclosure may apply a low level voltage to the second electrode E**2**. For example, the low level voltage line **200** may be electrically connected with the second electrode E**2** via connection electrodes **210** and **220**.

[0068] Also, a contact hole for exposing the low level voltage line **200** is provided in the buffer layer **120** and the intermediate insulating interlayer **130** according to one embodiment of the present disclosure, and the second electrode E**2** may be connected with the low level voltage line **200** via the connection electrodes **210** and **220** provided in the contact hole. The connection electrodes **210** and **220** may include the first connection electrode **210** being in contact with the low level voltage line **200**, and the second connection electrode **220** being in contact with the second electrode E**2**.

[0069] The first connection electrode **210** is provided in the same layer as the source/drain electrodes S/D, and is formed of the same material as that of the source/drain electrodes S/D. In this case, the source/drain electrodes S/D and the first connection electrode **210** may be manufactured at the same time by the same process, to thereby improve a manufacturing convenience.

[0070] The second connection electrode **220** is provided in the same layer as the first electrode E**1**, and is formed of the same material as that of the first electrode E**1**. In this case, the first electrode E**1** and the second connection electrode **220** may be manufactured at the same time by the same process, to thereby improve a manufacturing convenience.

[0071] The low level voltage line **200** according to one embodiment of the present disclosure is electrically connected with the second electrode E**2**, and the second electrode E**2** is electrically connected with the conductive layer **170** so that it is possible to reduce a resistance of the low level voltage line **200**. That is, as described above, the conductive layer **170** is formed in a pattern shape of a

material having high conductivity, and is then contact with the second electrode E2, whereby the resistance of the second electrode E2 may be lowered, and thus, a resistance of the low level voltage line **200** connected with the second electrode E2 may be also lowered. Even though there is an additional auxiliary line in the electroluminescent display device according to the first embodiment of the present disclosure, it is possible to reduce the resistance of the low level voltage line **200**. Thus, an area of the aperture portion AP may be increased by eliminating an occupied area required for the auxiliary line so that it is possible to improve an aperture ratio.

[0072] In case of the electroluminescent display device according to the first embodiment of the present disclosure, it is possible to keep the resistance of the low level voltage line (VSS) **200** in a low state, and also to improve uniformity of luminance by preventing non-uniformity of luminance over all of the pixels. Also, the auxiliary line is not required in the electroluminescent display device according to the first embodiment of the present disclosure so that it is possible to improve the aperture ratio, and also to ensure a long lifespan of the electroluminescent display device according to the first embodiment of the present disclosure.

[0073] The signal pad **300** is provided on the pad portion DP of the substrate **100**. The signal pad **300** is provided on the buffer layer **120**. The signal pad **300** according to one embodiment of the present disclosure may be formed of the same material as that of the gate electrode G of the active area AA. In this case, the signal pad **300** and the gate electrode G may be manufactured at the same time by the same process.

[0074] The pad electrode **310** is provided on the pad portion DP of the substrate **100**. The pad electrode **310** is provided on the insulating interlayer **130**, and is connected with the signal pad **300** via the contact hole.

[0075] The pad electrode **310** according to one embodiment of the present disclosure may be formed of the same material as those of the first connection electrode **210** and the source/drain electrodes S/D of the active area AA. In this case, the pad electrode **310**, the source/drain electrodes S/D and the first connection electrode **210** may be manufactured at the same time by the same process.

[0076] Additionally, a corrosion-resistant cover pad electrode may be provided on an upper surface of the pad electrode **310** according to one embodiment of the present disclosure. Thus, a lateral surface of the pad electrode **310** is covered by the passivation layer **140** so that it is possible to prevent the lateral surface of the pad electrode **310** from being corroded, and it is possible to prevent the upper surface of the pad electrode **310** from being corroded by the use of corrosion-resistant cover pad electrode.

[0077] FIG. **4** is a cross sectional view along I-I' of FIG. **2** according to the second embodiment of the present invention. The electroluminescent display device of FIG. **4** is obtained by changing a structure of a second electrode E2, whereby a detailed description for the same parts will be omitted, and only the different structures will be described in detail as follows.

[0078] Referring to FIG. **4** the electroluminescent display device according to the second embodiment of the present disclosure includes the second electrode E2.

[0079] The second electrode E2 is provided on an emission layer EL and a bank **160**. As the second electrode E2 is provided on a light emission surface, the second electrode E2 is formed of a transparent conductive material. However, the transparent conductive material has a relatively higher resistance than a metal material, a conductive layer **170** may be additionally provided so as to reduce the resistance of the second electrode E2.

[0080] The second electrode E2 according to one embodiment of the present disclosure may be provided on a aperture portion AP of a substrate **100**. In detail, the second electrode E2 may be formed in a pattern shape on the aperture portion AP of the substrate **100**. The second electrode E2 is patterned by each pixel, whereby the second electrode E2 is not directly connected with a low level voltage line **200**. The second electrode E2 is in contact with the conductive layer **170**, and is electrically connected with the conductive layer **170**, and the conductive layer **170** is electrically connected with the low level voltage line **200** via a contact hole, whereby the second electrode E2 and the low level voltage line **200** may be electrically connected with each other.

[0081] The low level voltage line **200** according to one embodiment of the present disclosure is provided on a low level voltage line contact portion CP of the substrate **100**. The low level voltage line **200** according to one embodiment of the present disclosure may be electrically connected to the conductive layer **170** via connection electrodes **210** and **220**.

[0082] Also, a contact hole for exposing the low level voltage line **200** is provided in a buffer layer **120** and an intermediate insulating interlayer **130** according to one embodiment of the present disclosure, and the conductive layer **170** may be connected with the low level voltage line **200** via the connection electrodes **210** and **220** provided in the contact hole.

[0083] The low level voltage line **200** according to one embodiment of the present disclosure is electrically connected to the conductive layer **170**, and the conductive layer **170** is electrically connected to the second electrode E2 so that it is possible to reduce a resistance of the low level voltage line **200**. That is, when the conductive layer **170** is formed in a pattern shape of a material having high conductivity, and is then electrically connected to the low level voltage line **200**, the resistance of the low level voltage line **200** may have relatively lowered resistance as compared to the resistance of the low level voltage line **200** on the direct contact between the low level voltage line **200** and the second electrode E2. That is, according as the conductive layer **170** formed in the plurality of pattern shapes is in contact with the second electrode E2, the resistance in the conductive layer **170** and the second electrode E2 is lowered. Thus, even though an additional auxiliary line is not provided in the electroluminescent display device according to the second embodiment of the present disclosure, it is possible to reduce the resistance of the low level voltage line **200**. Thus, an area of the aperture portion AP may be increased by eliminating an occupied area for the auxiliary line so that it is possible to improve an aperture ratio.

[0084] In case of the electroluminescent display device according to the second embodiment of the present disclosure, it is possible to keep the resistance of the low level voltage line **200** in relatively low state, and also to improve uniformity of luminance by preventing non-uniformity of luminance over all of the pixels. Also, the auxiliary line is not provided in the electroluminescent display device according to the second embodiment of the present disclosure so that it is possible to improve the aperture ratio, and

also to ensure a long lifespan of the electroluminescent display device according to the second embodiment of the present disclosure.

[0085] According to the embodiment of the present disclosure, it is possible to reduce the resistance of the low level voltage line by the use of conductive layer formed in the pattern shape on the second electrode, thereby improving the aperture ratio and ensure the long lifespan of the electroluminescent display device.

[0086] It will be apparent to those skilled in the art that the present disclosure described above is not limited by the above-described embodiments and the accompanying drawings and that various substitutions, modifications, and variations can be made in the present disclosure without departing from the spirit or scope of the disclosures. Consequently, the scope of the present disclosure is defined by the accompanying claims, and it is intended that all variations or modifications derived from the meaning, scope, and equivalent concept of the claims fall within the scope of the present disclosure.

[0087] The various embodiments described above can be combined to provide further embodiments. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety. Aspects of the embodiments can be modified, if necessary to employ concepts of the various patents, applications and publications to provide yet further embodiments.

[0088] These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

What is claimed is:

1. An electroluminescent display device comprising:

a substrate;

a first electrode provided on the substrate;

a bank covering an end of the first electrode and defining an emission area;

an emission layer provided on the first electrode in the emission area defined by the bank;

a second electrode provided on the emission layer and the bank;

a conductive layer provided on the second electrode; and

a low level voltage line provided on the substrate and electrically connected to at least one of the second electrode and the conductive layer.

2. The electroluminescent display device according to claim **1**, wherein the substrate includes an active area, and a non-active area surrounding the active area, the active area includes an aperture portion corresponding to the emission area, and a bank portion, and the non-active area includes a gate driver, a pad portion and a low level voltage line contact portion,

wherein the conductive layer is provided on the bank portion and the low level voltage line contact portion.

3. The electroluminescent display device according to claim **1**, wherein the conductive layer includes a reflective material.

4. The electroluminescent display device according to claim **2**, further comprising:

a planarization layer provided below the first electrode and a passivation layer provided below the planarization layer, wherein the planarization layer and the passivation layer include a contact hole therein.

5. The electroluminescent display device according to claim **4**, wherein the second electrode is provided at the active area and the low level voltage line contact portion.

6. The electroluminescent display device according to claim **5**, wherein the second electrode is connected with the low level voltage line via the contact hole.

7. The electroluminescent display device according to claim **4**, wherein the second electrode is provided at the aperture portion.

8. The electroluminescent display device according to claim **7**, wherein the second electrode is in contact with the conductive layer, and the conductive layer is connected with the low level voltage line via the contact hole.

9. An electroluminescent display device comprising:

a substrate where an active area and a non-active area are defined;

a first electrode disposed on the substrate;

a bank covering both lateral ends of the first electrode and defining an emission area which corresponds to an aperture portion of the active area;

a second electrode disposed on the emission layer and the bank;

an emission layer disposed between the first and second electrodes in the emission area defined by the bank;

a low level voltage line disposed at a low level voltage line contact portion of the non-active area and electrically connected to the second electrode; and

a conductive layer disposed on the second electrode and positioned at the bank portion and the low level voltage line contact portion.

10. The electroluminescent display device according to claim **9**, wherein the conductive layer includes a reflective material.

11. The electroluminescent display device according to claim **9**, further comprising a planarization layer disposed below the first electrode and a passivation layer disposed below the planarization layer,

wherein the planarization layer and the passivation layer have a contact hole.

12. The electroluminescent display device according to claim **9**, wherein the second electrode is disposed at the low level voltage line contact portion.

13. The electroluminescent display device according to claim **11**, wherein the second electrode is electrically connected with the low level voltage line through the contact hole.

14. The electroluminescent display device according to claim **9**, wherein the second electrode is disposed at the aperture portion.

15. The electroluminescent display device according to claim **13**, wherein the second electrode is in contact with the conductive layer and electrically connected with the low level voltage line through the contact hole.

16. An electroluminescent display device comprising:

a substrate where an active area and a non-active area are defined, wherein the active area includes an aperture portion and a bank portion, and the non-active area includes a gate driver, a pad portion and a low level voltage line contact portion;

a thin film transistor disposed at the aperture portion of the active area;

a passivation layer covering the thin film transistor and having first and second contact holes;

a first electrode disposed at the aperture portion and electrically connected to the thin film transistor through the first contact hole;

a bank covering both lateral ends of the first electrode and defining an emission area which corresponds to the aperture portion of the active area;

a second electrode disposed on the emission layer and the bank;

an emission layer disposed between the first and second electrodes in the emission area defined by the bank;

a low level voltage line disposed at a low level voltage line contact portion of the non-active area and electrically connected to the second electrode through the first contact hole; and

a conductive layer disposed on the second electrode and positioned at the bank portion and the low level voltage line contact portion.

17. The electroluminescent display device according to claim **16**, wherein the conductive layer includes a reflective material.

18. The electroluminescent display device according to claim **16**, further comprising a planarization layer disposed between the first electrode and the passivation layer having a third and fourth contact holes respectively connected to the first and second contact holes of the passivation layer.

19. The electroluminescent display device according to claim **16**, wherein the second electrode is disposed at the low level voltage line contact portion.

20. The electroluminescent display device according to claim **18**, wherein the second electrode is electrically connected to the low level voltage line through the second and fourth contact holes.

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申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
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摘要(译)

公开了一种电致发光显示装置，其能够克服与低电平电压线的电阻相关的问题而没有任何孔径比的损失，其中电致发光显示装置可以包括基板，设置在基板上的第一电极，构造的堤覆盖第一电极的一端并限定发光区域，设置在由堤岸限定的发光区域中的第一电极上的发光层，设置在发光层和堤岸上的第二电极，设置在其上的导电层第二电极和设置在基板上并与第二电极或导电层电连接的低电平电压线。